	L #	Hits	Search Text	DBs	Time Stamp
1	L1	1543	(halo or pocket) and ldd	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/29 13:50
2	L2	1377	source and drain and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/29 13:50
3	L3	584	dose and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/29 13:50

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	386	cmos and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/29 13:50
5	L5	373	4 and ((@ad<"20030923") or (@rlad<"20030923"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/29 13:51

DOCUMENT-IDENTIFIER: US 20030020125 A1

TITLE: InverseT- gate structure using damascene processing

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Application Filing Date - APD (1):
20010720

Summary of Invention Paragraph - BSTX (5):
[0004] Fabrication processes for metal oxide semiconductor field-effect transistors ("MOSFET") devices are well known. Gate structures for MOSFETs are generally manufactured by placing an undoped polycrystalline silicon ("polysilicon") layer over a relatively thin insulator ("gate oxide") layer. The gate oxide sits on a substrate having a well region. The polysilicon layer and the oxide layer are then patterned to form a gate conductor over the well region and the structure is subjected to implanted impurities to make selective regions conductive. Such implantation serves both to dope the gate conductor and to form lightly-doped regions ("**LDD**") in the silicon substrate.

Summary of Invention Paragraph - BSTX (6):
[0005] If the dopant species used is n-type, then the resulting MOSFET is typically an NMOS ("n-channel") transistor device. Conversely, if the dopant species is p-type, then the resulting MOSFET is typically a PMOS ("p-channel") transistor device. Integrated circuits typically use either n-channel devices exclusively, p-channel devices exclusively, or a combination of both on a single substrate. The combination of a n-channel device and a p-channel device on a single substrate is termed a complementary MOS ("**CMOS**") device. In such structures, one of the active regions, typically the region in which the p-channel device is to be formed, is covered with a masking layer. N-type dopants are implanted into the n-channel devices.

Summary of Invention Paragraph - BSTX (7):

[0006] After the first doping process, insulating sidewall spacers are formed on the sidewalls of the gate structure. A second implant **dose** is then forwarded into the gate structure and the silicon substrate. The second implant is done at a higher implant energy and **dose** than the first and creates **source/drain** regions within the silicon substrate. The gate conductor is preferably used to self-align the impurities implanted into the substrate to form the **source and drain** regions. The process is then repeated for the p-channel transistor, except now p-type dopants are implanted and the n-channel transistors are protected with a mask.

Summary of Invention Paragraph - BSTX (8):

[0007] It has been found advantageous to utilize a gate conductor that has the shape of an inverted "T" when viewed in a cross-section. Specifically, an inverse-T gate has a thick center section bordered by wings that are thinner. Such a structure allows a small portion of impurities to pass through the thinner outer portions (wings) of the inverted-T structure into the substrate while simultaneously blocking such impurities from the thicker main part of the gate conductor. Therefore, with an inverse-T gate structure, the **LDD** regions can be simultaneously formed with the heavily doped **source/drain** regions in a single doping process (as opposed to the two-stage doping process discussed above).

Summary of Invention Paragraph - BSTX (9):

[0008] Various methods of fabricating MOSFETs with inverse-T gate structures have been tried previously. For example, inverse-T shaped gates in MOSFETs are disclosed in U.S. Pat. No. 5,654,218 and U.S. Pat. No. 5,241,203, which are hereby incorporated by reference. U.S. Pat. No. 5,654,218 discloses a

process using an isotropic etch to undercut a first sacrificial layer to form the wing-type structures forming the gate conductor. Control of this undercutting and resulting dimensions are inadequate in view of the smaller dimension of such devices being used today. The U.S. Pat. No. 5,241,203 teaches of a timed etch to control thickness of the wing-structures forming the gate structure. Again, control of etching of these wing-structures is inadequate with today's ultra-small devices. Thickness variations of the wing structures result in varying concentration and depth of the lightly-doped-**drain** **(LDD) and halo** implants.

Summary of Invention Paragraph - BSTX (11):

[0010] As inverse-T gate conductors become smaller and smaller with advancing technology, these variations in the etching/undercutting processes produce inconsistencies beyond acceptable manufacturing tolerances. Therefore, there is a need for a new system/method of manufacturing inverse-T gate structures that does not rely upon an etching/undercutting process. Further, there is a need for a process which consistently manufactures inverse-T gate structures with the same size dimensions to ensure uniform doping of the **LDD** regions. The invention described below provides such a method/system.

Summary of Invention Paragraph - BSTX (14):

[0012] The invention describes a field effect transistor having a substrate with a well region, a **source** region and a **drain** region. Also included in the invention is a gate oxide above the well region and a gate conductor above the gate oxide. The gate conductor has an inner inverse-T structure and an outer conductive material different than the inner inverse-T structure. Further, the outer conductive material covers the top and sides of the inverse-T structure. The outer conductive material is preferably tungsten. Also, the outer

conductive material and the inverse-T structure are the same length along the gate oxide. The outer conductive material has an inverse-U shape that matches an outline of the inverse-T shape of the inner inverse-T structure. The inverse-T structure contains a center portion with a thickness greater than outer wing portions. The wing portions are a different conductive material than the center portion.

Summary of Invention Paragraph - BSTX (17):

[0015] The invention also forms an oxide layer on a substrate to form the underlying layer. Further, the invention implants an impurity into the substrate to form **source and drain** regions in the substrate adjacent the inverse-T gate conductor. The invention implants a single impurity and simultaneously forms lightly-doped-**drain and source** regions in the substrate under the wing portions and more heavily doped **drain and source** regions in the substrate adjacent the wing portions. Further, implanting the impurity into the substrate can be used to form a **halo** implant in the substrate under the inverse-T gate conductor. In addition, the inverse-T gate conductor has a center portion with a thickness greater than outer wing portions. The implanting process forms the **halo** implant in the substrate under the wing portions. The invention implants the impurity into the well region of the substrate through the opening in the mask. In the invention, the thickness of the conductor layer determines the thickness of the wing portions.

Summary of Invention Paragraph - BSTX (20):

[0018] The invention provides a new system/method of manufacturing inverse-T gate structures that does not rely upon an etching/undercutting process. Further, the invention consistently manufactures inverse-T gate structures with the same size dimensions to ensure uniform doping of the **LDD and halo** regions.

Detail Description Paragraph - DETX (3):

[0041] As inverse-T gate conductors become smaller and smaller with advancing technology, variations in the conventional etching/undercutting wing sizing processes produce inconsistencies beyond acceptable manufacturing tolerances. The invention described below provides a new system/method of manufacturing inverse-T gate structures that does not rely upon the conventional etching/undercutting process to determine wing thickness. Further, the invention consistently manufactures inverse-T gate structures with the same size dimensions to ensure uniform doping of the **LDD and halo** regions.

Detail Description Paragraph - DETX (12):

[0050] In FIG. 7, the spacers 70, 75 are removed using a solvent/etchant that selectively attacks oxide but does not substantially affect polysilicon or silicon nitride. In FIG. 7, once the spacers 70, 75 are removed, the inverse-T shape of the gate conductor 40, 80 can be more clearly seen. At this point in the processing, the invention implants an impurity 71. The impurity will be blocked by the thicker sections of the gate 80 but can pass through the thinner portion of the gate 40 (e.g., the wings of the inverse-T gate). The impurity 71 can be a **halo** implant and/or **LDD** implant, the polarity of which will be determined by the type of transistor being manufactured. The **halo** implant may also include carbon for the purpose of containing a boron **halo** implant in an NFET device. The impurity implant process produces **LDD** implant regions 90, 95, and **halo** implant regions 97, 99 as shown in FIGS. 7-10. Implants are normal to the surface and do not require a "groundrule" limitation for adjacent topography as would angled implants to avoid shadowing. Providing normal implants does not limit scaling to smaller dimensions as would angled implants.

Detail Description Paragraph - DETX (14):

[0052] In FIG. 9, the silicon nitride 50 is selectively removed and the polysilicon layer 40 which exists outside the dimensions of the gate conductor is also removed (again, using a well known selective removal process). At this point, a number of alternatives are available, dependent upon the specific nature of the transistor being manufactured. For example, if the **LDD** implant was not made previously, it can be made now. Alternatively, the heavier **source/drain** implant can be performed at this time. In any manner, once the **source/drain** (main and **LDD**) implants are performed, the **source/drain** regions 130 are completed and shown in FIG. 10.

Detail Description Paragraph - DETX (15):

[0053] Conventional well-known processes are then utilize to complete the gate conductor structure. More specifically, the outer edge of the gate conductor is silicided 120. Additionally, insulating spacers 140 (which can be used to pattern the **LDD** implant differently from the main **source/drain** implant) are also formed. In addition, the gate cap 110 can be replaced with a more suitable material, if desired.

Detail Description Paragraph - DETX (16):

[0054] An important advance made by the invention is the ability to utilize a different material for the center 80 and wings 40 of the underlying inverse-T gate conductor. With the processing described above, the impurities within the gate conductor 40, 80 can be selectively applied at many points in the process. For example, directly after the polysilicon 40 is deposited in FIG. 1, some form of implant may be performed. Similarly, at the point in processing shown by FIG. 6, additional gate impurities may be implanted into the gate material 80. Cap 110 provides for separately doping gate 40, 80 and **source drain** regions 130, substantially avoiding implant for **source/drain** regions 130 from

getting into gate conductor 40, 80. Thus, the amount of doping received by the gate conductor and even the type of impurity utilized for the gate conductor is independent of the impurities utilized for the **source/drain** structures 130. Also, because of hard mask layer 50, the **source drain** is protected during implant of gate conductor 40, 80, so **source drain** doping is independent of the impurities used for doping the gate.

Detail Description Paragraph - DETX (19):

[0057] One of the principal advantages of the invention is the flexibility it provides to the engineer when designing such an inverse-T gate transistor. However, in a preferred embodiment, the inverse-T portion of the gate conductor 40, 80 would be formed of a doped polysilicon and the sides and top 100 of the gate conductor would be pure tungsten. The implant made in the processing shown in FIGS. 7-10 would comprise the **LDD** implant 90, 95 or **halo** implant 97, 99, or both. The heavier **source/drain** implants 130 would be made after the formation of the sidewall spacers 140. In this preferred embodiment, the **halo** implant 97, 99 would be precisely self-aligned with the wings 40 of the inverse-T portion of the gate conductor (in the processing shown in FIG. 7). Further, because the **halo** implant is not angled, its location and position can be precisely controlled with the invention. Additionally, as mentioned above, the thickness of the wings 40 is very easily controlled with the invention through the deposition of the polysilicon layer 40 in the processing shown in FIG. 1. Therefore, the invention is dramatically superior to conventional inverse-T gate manufacturing methodologies.

Detail Description Paragraph - DETX (25):

[0063] After the gate oxide 260 is formed, the gate conductor material 270 (polysilicon) is deposited over the structure and selectively etched below the

level of the silicon nitride pad 210. The silicon nitride pad 210 is then
subsequently removed, as shown in FIG. 18. Then, the spacers 250 are removed,
revealing the inverse-T gate structure shown in FIG. 19. The outer surface of
the inverse-T gate structure is silicided 275, using well known silicide
processing. In addition, the conventional **halo/LDD** implants 291 are performed,
as discussed above, to form the **source/drain** regions 290 and optional **halo**
regions.

Detail Description Paragraph - DETX (29):

[0067] As inverse-T gate conductors become smaller and smaller with
advancing technology, these variations in the etching/undercutting processes
produce inconsistencies beyond acceptable manufacturing tolerances. The
invention provides a new system/method of manufacturing inverse-T gate
structures that does not rely upon an etching/undercutting process nor does it
recap on angled implants under the wings. Further, the invention consistently
manufactures inverse-T gate structures with the same size dimensions to ensure
uniform doping of the **LDD and halo** regions.

Claims Text - CLTX (2):

1. A method of fabricating a gated device, comprising the steps of: a)
providing an active area in a semiconductor substrate; b) forming a temporary
layer on said active area; c) opening a window in said temporary layer above
said active area; d) forming a gate electrode in said window, wherein said
gate electrode has a first region having a first thickness and a second region
having a second thickness less than said first thickness; and e) implanting
with a vertical implant to provide a first **dose** to said substrate under said
first region and a second **dose** to said substrate under said second region,
wherein said first **dose** is less than said second **dose** and wherein said implant

is substantially vertical.

Claims Text - CLTX (9):
8. The method as recited in claim 7, wherein said doping is for providing an extension implant or a **halo** implant.

Claims Text - CLTX (14):
13. The method as recited in claim 12, wherein said dopant comprises one of a **halo** implant and a **source/drain** implant.

Claims Text - CLTX (23):
22. The method as recited in claim 21, wherein said implant provides a lightly doped **drain** region or a **halo** region.

Claims Text - CLTX (24):
23. The method as recited in claim 21, wherein said implant provides a lightly doped **drain** region and a **halo** region.

Claims Text - CLTX (25):
24. The method as recited in claim 1, wherein said implanting step (e) also provides **source/drain** doping.

Claims Text - CLTX (28):
27. The method as recited in claim 1, wherein a center portion of a channel or well under said gate electrode receives a **dose** different than edge portions of said channel or well.

Claims Text - CLTX (32):
31. The method as recited in claim 1, wherein implants for **halo and Ldd** are substantially vertical.

Claims Text - CLTX (40):
39. The method as recited in claim 1, wherein said implanting step provides a **dose** in said gate electrode and a **dose** in a channel under said gate electrode for an extension or a lightly doped **drain**.

Claims Text - CLTX (41):
40. The method as recited in claim 39, further comprising providing a **source/drain** doping in said single implanting step.

Claims Text - CLTX (42):
41. The method as recited in claim 39, further comprising providing a second implanting step for a **halo**.

Claims Text - CLTX (44):
43. A semiconductor structure as recited in claim 42 wherein said implanted region comprises a **source/drain, an LDD,** an extension, or a **halo**.

Claims Text - CLTX (45):
44. The structure as recited in claim 42, wherein said gate is implanted with a **dose** in a 1 E 14 cm-2 range and said **source/drain** is implanted with a **dose** in a 1 E 13 cm-2 range.

Claims Text - CLTX (46):
45. The structure as recited in claim 42, wherein said gate implant energy is in a 20 keV range and said **source/drain** implant energy is in a 10 keV range.

Claims Text - CLTX (58):
57. The semiconductor device in claim 53, wherein the device further comprises a **source/drain** diffusion and said gate conductor comprises a gate of an FET.

Claims Text - CLTX (59):
58. A field effect transistor comprising: a substrate comprising a channel, a **source** on one side of said channel, and a **drain** on an opposite side of the said channel; and a gate dielectric on said channel; and a gate conductor on said gate dielectric; wherein said gate dielectric includes a center portion and an edge portion, wherein said center portion is thinner than said edge portion.

Claims Text - CLTX (65):
64. The method in claim 63, further comprising implanting an impurity into said substrate to form **source and drain** regions in said substrate adjacent said inverse-T gate conductor.

Claims Text - CLTX (66):
65. The method in claim 64, wherein said inverse-T gate conductor comprises a center portion having a thickness greater than outer wing portions, and wherein said implanting an impurity step comprises a blocking implant in said center portion, providing a first doping in said substrate under said wing portions and a second doping beyond said wing portions for said **source and drain** regions, wherein said first doping is less than said second doping.

Claims Text - CLTX (67):
66. The method in claim 62, wherein said inverse-T gate conductor comprises a center portion having a thickness greater than outer wing portions, further comprising implanting an impurity into said substrate to form a **halo** implant in said substrate under said wing portions.

Claims Text - CLTX (73):
72. The method in claim 70, further comprising implanting an impurity into said substrate to form **source and drain** regions in said substrate adjacent said conductor.

Claims Text - CLTX (74):
73. The method in claim 72, wherein said conductor comprises an inverse-T gate conductor having a center portion having a thickness greater than outer wing portions and wherein said implanting process comprises a single impurity implant and simultaneously forms lightly-doped **drain and source** regions in said substrate under said wing portions and more heavily doped **drain and source** regions in said substrate adjacent said wing portions.

Claims Text - CLTX (75):
74. The method in claim 69, further comprising implanting an impurity into said substrate to form a **halo** implant in said substrate under said conductor.

Claims Text - CLTX (76):

75. The method in claim 74, wherein said conductor comprises an inverse-T gate conductor having a center portion having a thickness greater than outer wing portions and wherein said implanting process forms said **halo** implant in said substrate under said wing portions.